v02.0709

HMC706LC3C

13 Gbps, NRZ-to-RZ CONVERTER, +3.3V SUPPLY

Typical Applications

The HMC706LC3C is ideal for:

- NRZ-to-RZ data type conversion
- SONET OC-192 applications and equipment
- Mach-Zehnder optical modulator drivers
- Broadband test & measurement

Features

Supports High Data Rates: up to 13 Gbps

Differential & Single-Ended Operation

Fast Rise and Fall Times: 15 / 13 ps

Low Power Consumption: 594 mW typ.

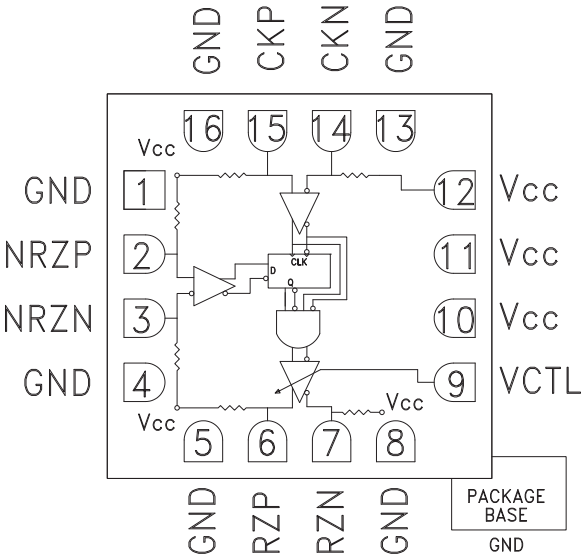
Programmable Differential
Output Voltage Swing: 300 - 1200 mV

Propagation Delay: 275 ps

Single Supply: +3.3V

16 Lead Ceramic 3x3mm SMT Package: $9mm^2$

Functional Diagram



General Description

The HMC706LC3C is a NRZ-to-RZ converter designed to support data transmission rates of up to 13 Gbps, and clock frequencies as high as 13 GHz. During normal operation, RZ data is transferred to the outputs on the positive edge of the clock. Reversing the clock inputs allows for negative-edge triggered applications. All input signals to the HMC706LC3C are terminated with 50 Ohms to Vcc on-chip, and may be either AC or DC coupled.

The differential outputs of the HMC706LC3C may be either AC or DC coupled. Outputs can be connected directly to a 50 Ohm Vcc terminated system, while DC blocking capacitors may be used if the terminating system is 50 Ohms to a non-Vcc DC voltage. The 50 Ohm termination resistors are bypassed on chip from Vcc to ground. The HMC706LC3C operates from a single +3.3V DC supply and is available in a ceramic RoHS compliant 3x3 mm SMT package.

Electrical Specifications, T_A = +25°C, Vcc = +3.3V

Parameter	Conditions	Min.	Typ.	Max	Units
Power Supply Voltage		3.0	3.3	3.6	V
Power Supply Current			180		mA
Maximum Data Rate			13		Gbps
Maximum Clock Rate			13		GHz
Input High Voltage		Vcc -0.5		Vcc +0.5	V
Input Low Voltage		Vcc -1.1		Vcc	V
Input Return Loss	Frequency <13 GHz		12		dB
Input Ampliftude	Single-Ended, peak-to-peak	50		1200	mVp-p
	Differential, peak-to-peak	100		2000	mVp-p
Adjustable Output Amplitude	Single-Ended, peak-to-peak	150		600	mVp-p
	Differential, peak-to-peak	300		1200	mVp-p
Output High Voltage			3.28		V

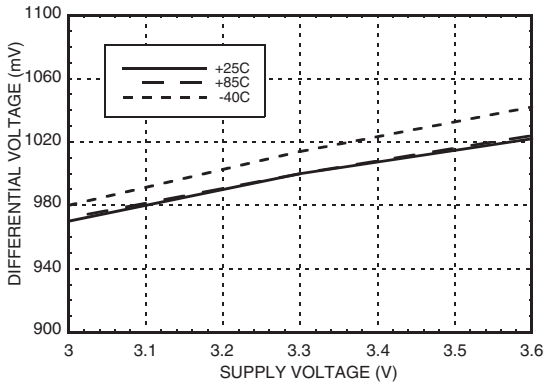
Electrical Specifications, (continued)

Parameter	Conditions	Min.	Typ.	Max	Units
Output Low Voltage			2.76		V
Output Rise / Fall Time	Differential, 20% - 80%		15 / 13		ps
Output Return Loss	Frequency <13 GHz		13.5		dB
Random Jitter Jr	rms [1]			0.2	ps rms
Deterministic Jitter, Jd	peak-to-peak, 2^{31}-1 PRBS input [2]		2		ps, p-p
Propagation Delay Clock to Data, td			275		ps
Clock Phase Margin	13 GHz		270		deg

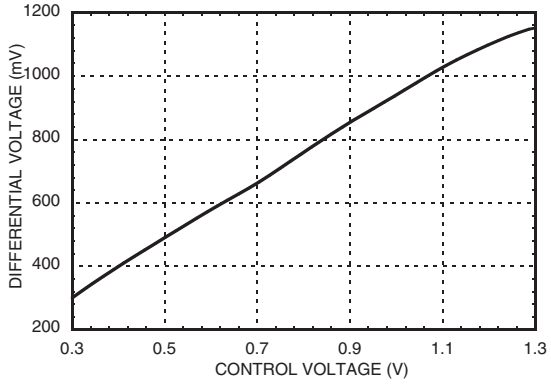
[1] Measured at 12.5 Gbps continuous 1010.... input pattern.

[2] Deterministic jitter calculated by simultaneously measuring the edge by edge variation of the output data stream with respect to the input clock.

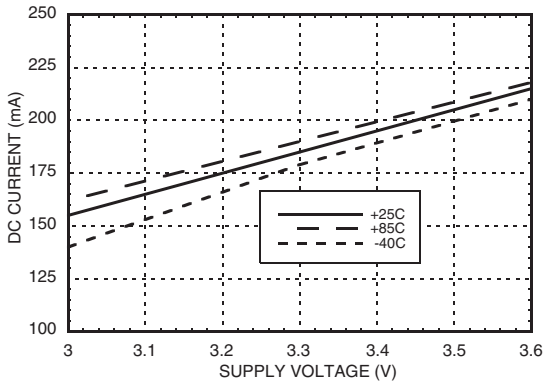
Differential Output Voltage vs. Supply Voltage [1]



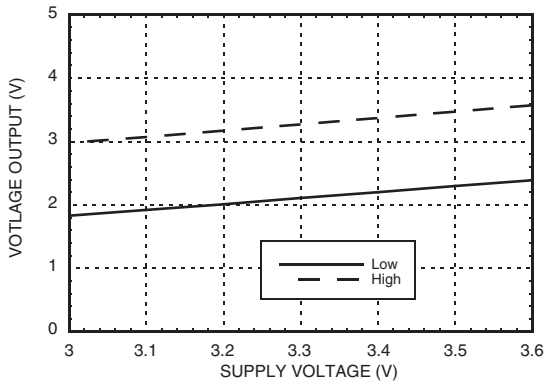
Differential Output Voltage vs. Control Voltage



DC Current vs. Supply Voltage [1]

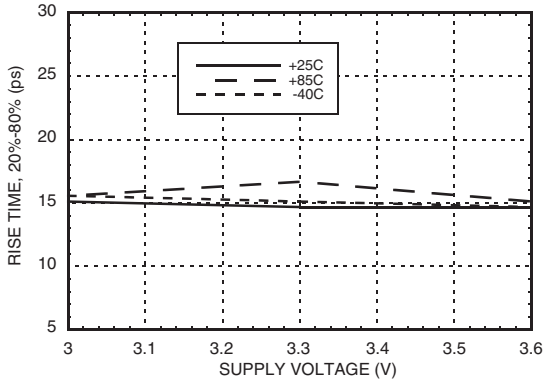


Output Low Voltage, Output High Voltage vs. Supply Voltage [1] [2]

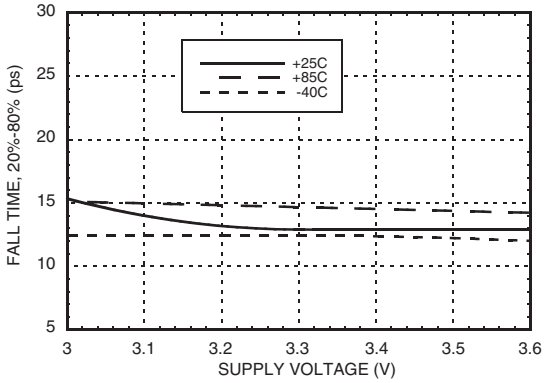


[1] Vctl = 1.1V [2] Frequency = 13 GHz

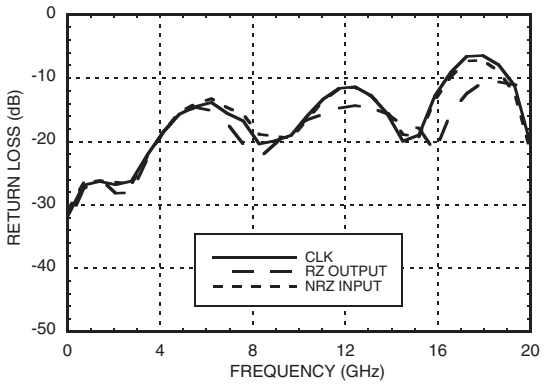
Rise Time vs. Supply Voltage [1] [2]



Fall Time vs. Supply Voltage [1] [2]

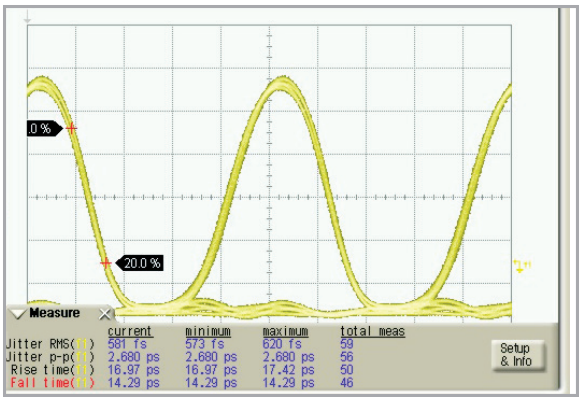


Return Loss



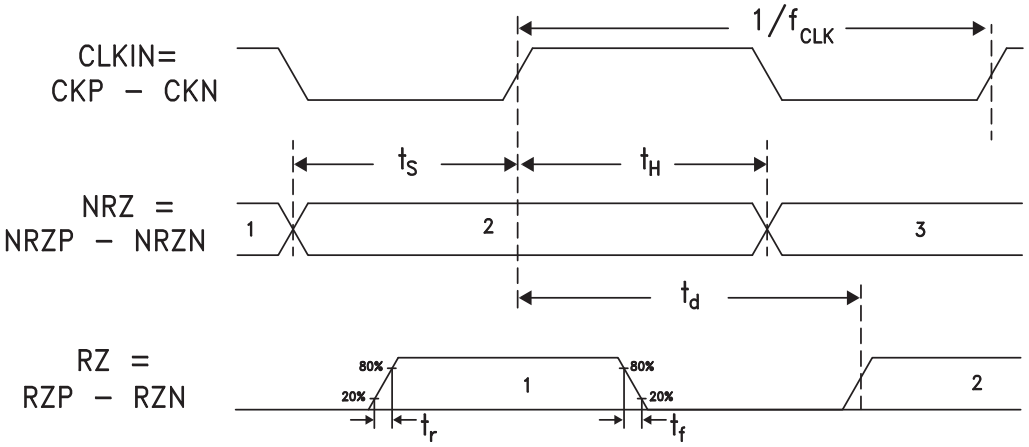
[1] Vctl = 1.1V [2] Data Rate = 13 Gbps

Eye Diagram [1]



[1] Test Conditions:
Eye diagram data presented on an Infinium DCA 86100A
Rate = 10.0 GB/s
Pseudo Random Code = 2^{31} -1
Vin = 400 mVp-p differential

Timing Diagram



t_S = Set Up Time

t_h = Hold Time

t_d = Propagation Delay

$t_C = \frac{1}{f_{CLK}}$

$t_{SH} = t_s + t_h$

CPM = Clock Phase Margin = $360° \frac{t_C - t_{SH}}{t_C}$

Truth Table

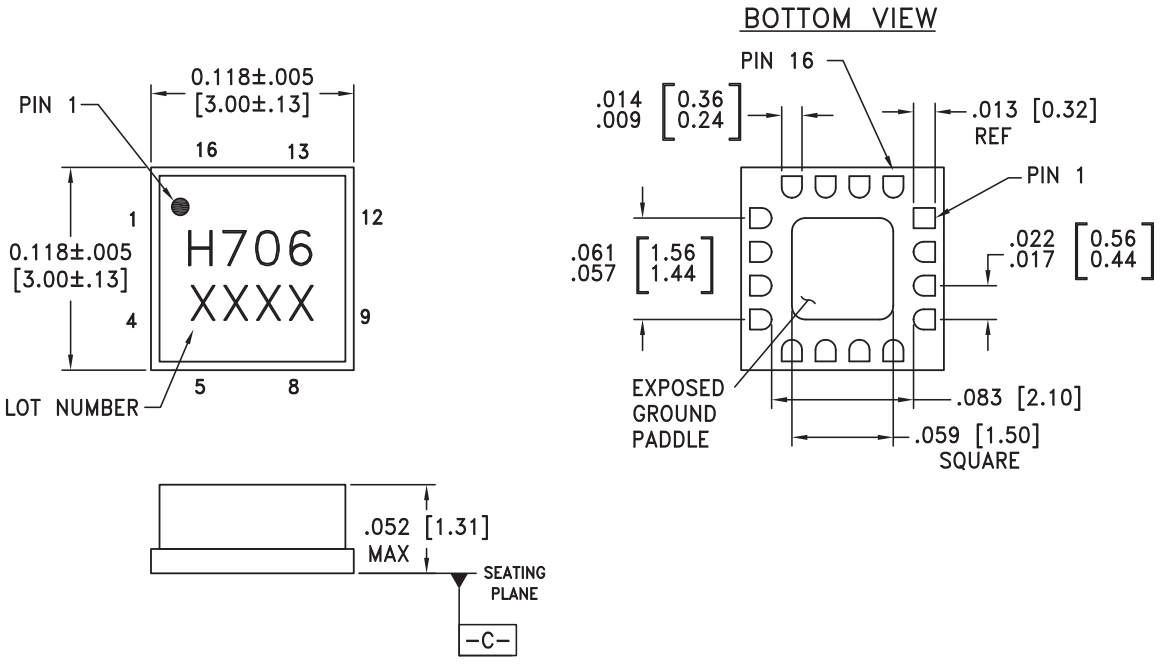
Input		Outputs
D	C	Q
L	L -> H	L
H	L -> H	H
X	H -> L	L
Notes: D = DP - DN C = CP - CN Q = QP - QN	H - Negative voltage level L - Positive voltage level	

Absolute Maximum Ratings

Power Supply Voltage (Vcc)	-0.5V to +3.6V
Input Signals	Vcc - 2V to Vcc + 0.5V
Output Signals	Vcc -1.5V to Vcc +1.0V
Storage Temperature	-65°C to +150°C
Operating Temperature	-40°C to +85°C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

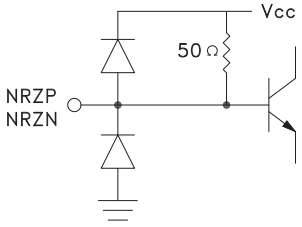
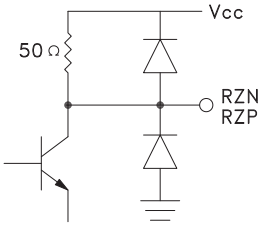
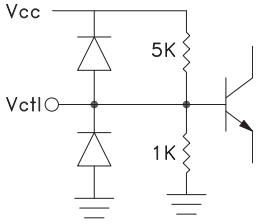
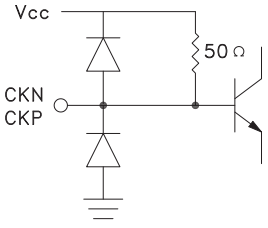
Outline Drawing



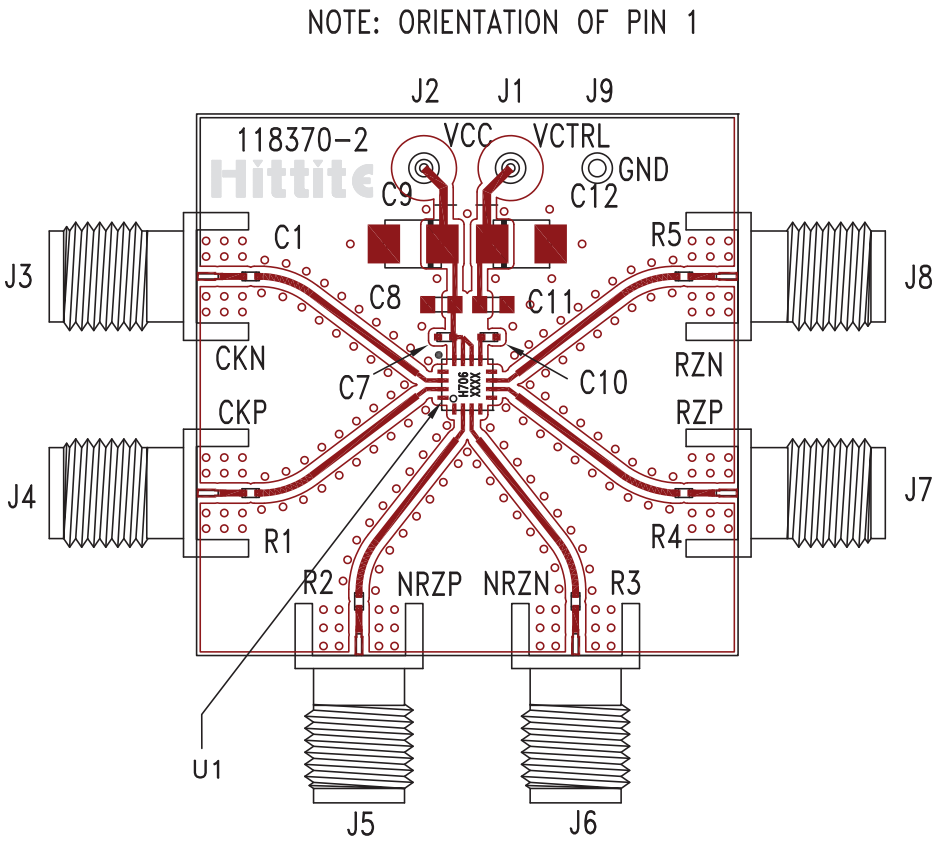
NOTES:

1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING:
   30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. GROUND PADDLE MUST BE SOLDERED TO GND.

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 4, 5, 8, 13, 16 Ground Paddle	GND	Signal & Supply Ground	
2, 3	NRZP, NRZN	NRZ Data Inputs	
6, 7	RZP, RZN	RZ Data Outputs	
9	Vctl	Output Level Control	
10 - 12	Vcc	Positive Supply	
14, 15	CKN, CKP	Clock Inputs	

Evaluation PCB



List of Materials for Evaluation PCB 118372 [1]

Item	Description
J1, J2, J9	DC Pin
J3 - J8	K Connector
C1	10 pF Capacitor, 0402 Pkg.
C7	1 nF Capacitor, 0402 Pkg.
C8, C11	100 nF Capacitor, 0603 Pkg.
C9, C12	4.7 µF Case A, Tantalum
C10	100 pF Capacitor, 0402 Pkg.
R1 - R5	0 Ohm Resistor, 0402 Pkg.
U1	HMC706LC3C High Speed Logic, NRZ to RZ Converter
PCB [2]	118370 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR, FR4

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed package base should be connected to ground. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Application Circuit